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# Transparent Resilience for Approximate DRAM

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#### Approximate Computing

- Explores the inaccuracy tolerance of applications
- Obtain energy efficiency at the cost of errors
- Several computation can tolerate errors

Original image









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### Problem Statement

- Uncontrolled errors lead to execution crashes
- Execution crashes cause output data loss
  - Wasting of computational efforts
  - Reduce energy savings
- All applications have critical data
- Invalid results can be generated
  - We need to recover these results





#### Approximate DRAM



Relative energy consumption on memory hierarchy

- Adjusting operational parameters
- Bitflips affect stored data



Adapted from: Yarmand et al. (2019).







Error rate of MT47H32M8 on different refresh rates

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#### Non-Transparent Interfaces

• EnerJ (<u>Sampson *et al.*, 2011</u>)

• Relax (<u>De Kruijf *et al.*, 2012</u>)

```
@Approx class Mean {
@Precise int length_sample;
public float calculate(@Approx int[] nums) {
  @Approx float total = 0.0f;
  for (@Precise int i=0; i<length_sample; i++)
      total += nums[i];
  return total / length_sample;
}</pre>
```



#### Transparent Interfaces

- Act based on general behavior of applications
- Crash Skipping (Verdeja Herms & Li, 2019)
  - Replaces instructions that would crash execution by a "nop"
- AxRAM (Fabrício Filho et al., 2020)
  - Protects common critical data regions
  - Application stack: usually small region
  - Validate memory instructions
  - Truncate memory references into allowed boundaries





#### Transparent Interface Design

- AxRAM mitigates data crashes
  - Caused by wrong fetched addresses
- Crash Skipping (CSi) mitigates flow crashes and execution stalling
  - Interruptions in the control flow
  - Counters of avoided crashes
- We propose a merge of these characteristics to model a single interface that avoids these three types of crashes







#### Transparent Resilience for Approximate DRAM

- Approximate DRAM mitigates a more energy-intensive point of the memory hierarchy
- Restarting invalid executions
  - Execution crashes are easily detected by an OS
  - Silent Data Corruptions (SDC) generate invalid output not easily detected
- Acceptance tests may detect invalid outputs generated by SDC

#### **Transparent Re-execution**

- Accurate re-execution
  - Generates a valid and accurate output
  - Nullifies the energy gains of the current instance
- Approximate re-execution
  - A new invalid output may be generated
- Proposal: approximation levels
  - Re-execution with lower error probability



### Software-Level Addressing Scheme

- AxRAM validates memory addresses into allowed boundaries
- Virtual addressing is not as simple as direct addressing
  - Truncating addresses does not validate the existence of a valid virtual page
- Searching for a valid Page Table Entry (PTE)
  - Starts from the higher level of the Virtual Page Number (VPN)
  - Search for a VPN with hamming distance=1 with the wrong address
  - If a correspondence is found, a new PTE is created to the same physical address

#### Simulation Tools and Models

- Approximate DRAM levels:
  - Voltage ranging from 1.02 to 1.11V with 10mV steps



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#### Frequencies of Quality and Crashes

resilience mechanisms tends to insist on executions with error, thus increasing invalid results without crashing







#### with transparent resilience





atax

sobel

#### Acceptance Tests



#### Approximate Re-execution



dijkstra atax 100.0% 100.0% 95.0% 95.0% Expected Quality Expected Quality 90.0% Expected Quality 90.0% 85.0% 85.0% 80.0% 75.0% 80.0% 70.0% 75.0% 65.0% 60.0% 70.0% 1.08 1.09 1.08 1.09 1.10 1.11 1.07 1.10 1.11 1.07 vdd vdd



#### Interfaces and Stack Protection achieve higher quality with stack correlation achieves higher protection savings and quality protecting application stack Expected Quality Expected Energy Savings 100% 99.0% 98.6%) 98.5% 100.0% 35.0% 30.5% 30.6% 30.0% 95.0% 25.0% 90.0% 20.0%) 19.3% 20.0% 17.8% 85.0% 15.0% 10.0% 80.0% 10.0% 74.9% 75.0% 5.0% 71.6% 0.0% 70.0% correlation correlation dijkstra sobel dijkstra sobel stack no stack stack no stack dijkstra has no benefits on protecting application stack 15

sobel has a slight impact on energy to



On lower vdds, AxRAM achieves higher energy savings and SW-AC follows this trend and occasionally surpasses these benefits On applications that have no benefits on protecting addresses and stack, SW-ACw follows the benefits of CSi due to the lower overhead On higher vdds, CSi has the lower overhead due to less protections and SW-ACw achieves closer energy savings

SW-AC and SW-ACw achieve higher

savings on lower and higher vdds,

## Final Remarks

- Approximate DRAM
  - Less impact of error in application and higher energy savings
- Acceptance tests
  - Detects invalid results even with SDC
  - Improve detection up to 30%
- Approximate Re-execution
  - Up to 4p.p. of energy with negligible loss in quality
- Combined interface mechanisms
  - Lower overhead of CSi with lower error rate
  - Higher safeguard of AxRAM with higher error rate
- Transparent interfaces mechanisms
  - Improve execution resilience without changes in the source code
  - Increase average quality and energy savings among several approximation levels

## Thanks!

## Questions?

More information: <u>http://varchc.github.io/arcs</u>

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